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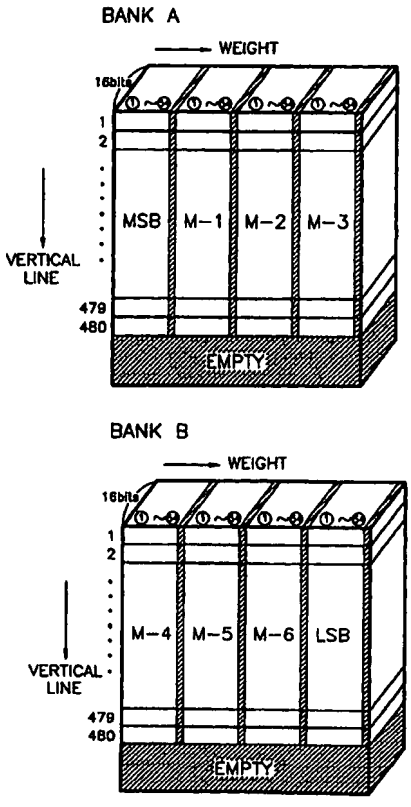
(54) Title: METHOD OF PROCESSING VIDEO DATA IN PDP TYPE TV RECEIVER

(57) Abstract

A method of writing N/K groups of non-interlaced video data and reading the same, in/from SDRAM used as a frame memory in a PDP type TV receiver, where one frame comprises N x M pixels, each of pixels being sampled with L bits, and then K samples are reordered by L number of weight data and reading the same is described. First, a first bank of the SDRAM is divided into L/2 number of column regions for storing upper L/2 number of weight data according to weights, respectively. Second, a second bank of the SDRAM is divided into L/2 number of column regions for storing lower L/2 number of weight data according to their weight, respectively. Third, the N/K groups of non-interlaced video data corresponding to M vertical line are written into respective column regions in M row of the first and second banks according to the weights, wherein N is the number of horizontal pixels, M is the number of vertical lines, L is the number of subfields, and K is the number of bits of the weight data. Accordingly, in writing the video data based on the non-interlaced scanning method on a frame memory using the SDRAM which is relatively cheap and reading the video data from the frame memory, since a burst write or burst read operation is allowed, the configuration of the write or read address generator can be simplified.



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METHOD OF PROCESSING VIDEO DATA IN PDP TYPE TV RECEIVER

DESCRIPTION

TECHNICAL FIELD OF THE INVENTION

The present invention relates to a method of processing video data in a plasma display panel (PDP) type TV receiver, and more particularly, to a method of rearranging video data sampled in 8 bits into units of 8 bits or 16 bits according to weight, writing the rearranged video data on a synchronous random access memory (SDRAM) and reading the same.

BACKGROUND ART

For attaining high-resolution vivid picture image in a display device for home-use, such as a television receiver, a large-scale display having a size of 50 inches or a small-sized display device which does not occupy a large area is increasingly demanded. In order to satisfy such a demand, recently, much attention has been paid to a flat type display device such as a liquid crystal display (LCD), a PDP, a flat-cathode ray tube or an electrioluminescent panel (ELP). However, it is not easy to fabricate a large-scale LCD and an ELP having a full-color display feature. The PDP having a thickness of approximately 3 cm for forming a picture image using luminescence due to a gas discharge is advantageous in terms of full-color and large-scale display and is applicable to wide fields including medium-, large- and superlarge-sized display devices. In particular, the PDP stands unchallenged in the field of a self-emission type large-scale HDTV displays. The PDP is classified into an alternating current (AC) type, a direct current (DC) type and an AC-DC hybrid type depending on its structural features and a difference between voltages applied thereto. Among these PDPs, since the AC-type PDP is completely digitized in terms of its driving characteristics, it is noted as a next-generation display in which a television and a personal computer are combined.

FIG. 1 shows a general AC-type color PDP-TV receiver. An audio/video portion **114** separates R.G.B analog signal and horizontal and vertical synchronization signals from a National Television System Committee (NTSC) composite video signal received through an antenna **112**, obtains an average picture

level (APL) corresponding to the average of brightness signals (Y) to then supply the obtained APL to an analog/digital converter **116**. The received NTSC composite video signal based on an interlaced scanning method is composed of frames, each frame consisting of two fields, that is, an odd field and an even field. The analog/digital converter **116** receives the R.G.B analog signal and converts the same into R.G.B digital signal. An interlaced/non-interlaced scan converter **117** converts the R.G.B digital signal based on an interlaced scanning method into a video signal based on a non-interlaced scanning method to then output the converted R.G.B data to a memory unit **118**. The memory unit **118** reconfigures one-field video data into a plurality of subfields for PDP gray-scale processing and then rearranges the same from the most significant bit (MSB) to the least significant bit (LSB), which will be described in more detail with reference to FIG. 2.

In FIG. 2, the memory unit **118** includes a data rearrangement portion **210**, an address generator **220**, a control clock generator (not shown), first and second frame memories **230** and **240**, and a data selector **250**. The data rearrangement portion **210** includes first and second shift registers **211** and **212**, a D flip-flop & multiplexer **213**, and first and second tri-state buffers **214** and **215**, and rearranges the video data supplied in parallel, that is, from the MSB to the LSB, from the audio/video converter **116** so as to be stored as bits having the same weight in one address of the first and second frame memories **230** and **240**. In other words, the first shift register **211** and the second shift register **212** alternately repeat a load operation and a shift operation to classify the sampled video data according to their weights. While the first shift register **211** loads 16 sampled video data, the second shift register **212** sequentially shifts 16 previously loaded video data and outputs the same. Also, while the first shift register **211** shifts the loaded video data according to their weights and outputs the same, the second shift register **212** loads 16 sampled video data again. Here, while the shifter register performing the load operation loads 16 video data, the shift register performing the shift operation shifts the video data 8 times. For better driving of the shift register, the input clock frequency is made to be double the output clock frequency. The D flip-flop & multiplexer **213** selects the data having the same weight output from either the first shift register **211** or the second shift register **212**, whichever operating in a shift mode, and supplies the

selected data to the first and second tri-state buffers **214** and **215**. The first and second tri-state buffers **214** and **215** supply the rearranged video data supplied from the D flip-flop & multiplexer **213** to the first or second frame memory **230** or **240**, whichever operating in a write mode.

Generally, a PDP type TV receiver having an aspect ratio of 16:0, in which one- frame video data is approximately 10 Mbits, that is, 853 × 3 (R, G, B) × 480 × 8 (bits), alternately performs a write operation and a read operation in units of frames using the first and second frame memories **230** and **240** having a 10 Mbit memory capacity.

The address generator **220** includes a write address generator **221** and a read address generator **222**, generates addresses of data stored in the first or second frame memory **230** or **240** and supplies the generated addresses to the first or second frame memory **230** or **240**. For PDP gray-scale processing, all of the video data constituting one frame are divided into subfields according to their weights. During the read operation, the video data corresponding to the respective frames are sequentially read to then be supplied to a data interface unit **120** (FIG. 1). Thus, the write address generator **221** and the read address generator **222** operate in a different manner.

The address selector **223** supplies the corresponding addresses to the first and second frame memories **230** and **240** according to the respective operation modes of the first and second frame memories **230** and **240**, that is, a write mode or a read mode. The data selector **250** selects the video data output from the first or second frame memory **230** or **240**, whichever operates in the read mode, and supplies the selected video data to the data interface unit **120**.

Referring back to FIG. 1, the data interface unit **120** temporarily stores the R.G.B data supplied from the memory unit **118** and supplies the same to first and second address driver ICs **130** and **132** in conformity with a data format requested by the first and second address driver ICs **130** and **132**. In other words, the R.G.B data output from the memory unit **118** are rearranged according to the R.G.B pixel arrangement principle of a PDP **134** to then be output to the first and second address driver ICs **130** and **132**. The data interface unit **120** requires a space for temporarily

storing data corresponding to 2 lines, that is, 640 lines × 3 (R, G, B) × 2 = 3840 (bits). Here, while the data corresponding to one line are input, the data corresponding to the other line are alternately output.

A high voltage driver circuit **126** combines DC voltages supplied from an AC/DC converter **124** according to logic control pulses output from a timing controller **122** and generates high voltage control pulses required by a scan/sustain driver IC **128** to then drive the PDP **134**. Also, data streams supplied from the data interface unit **120** to the first and second address driver ICs **130** and **132** are turned to appropriately high voltage levels so as to be selectively written on the PDP **134**.

As described above, the method of storing a video signal in a memory for displaying a picture image on a PDP may vary according to kinds of memories. Here, the memories are classified into DRAMs, SRAMs, SDRAMs and so on. Accordingly, it is necessary to write and read a video signal on and from the RAM in a different manner depending on the kinds of the memories.

DISCLOSURE OF THE INVENTION

To solve the above problems, it is an object of the present invention to provide a method of writing and reading a video signal on and from a frame memory using a synchronous dynamic random access memory (SDRAM) in a PDP type TV receiver.

Accordingly, to achieve the above object according to a first embodiment of the present invention, there is provided a method of writing N/K groups of non-interlaced video data in an SDRAM used as a frame memory in a PDP type TV receiver, where one frame comprises N × M pixels, each of pixels being sampled with L bits, and then K samples are reordered by L number of weight data, comprising the steps of: a) dividing a first bank of the SDRAM into L/2 number of column regions for storing upper L/2 number of weight data according to weights, respectively; b) dividing a second bank of the SDRAM into L/2 number of column regions for storing lower L/2 number of weight data according to the weight, respectively; and c) writing the N/K groups of non-interlaced video data corresponding to M vertical line into respective column regions in M row of the first and second banks according to the weights, wherein N is the number of horizontal

pixels, M is the number of vertical lines, L is the number of subfields, and K is the number of bits of the weight data.

T achieve the above object according to a first embodiment of the present invention, there is provided a method of reading N/K groups of non-interlaced video data in an SDRAM having a first bank including L/2 number of column regions for storing upper L/2 number of weight data according to weights and a second bank including L/2 number of column regions for storing lower L/2 number of weight data according to weights, used as a frame memory in a PDP type TV receiver, where one frame comprises N × M pixels, each of pixels being sampled with L bits, and then K samples are reordered by L number of weight data, comprising the steps of: a) reading respective weight data from the L/2 number of column regions of the first bank according to the weights and vertical lines so as to forming upper L/2 number of subfields for M number of vertical lines; and b) reading respective weight data from the L/2 number of column regions of the second bank according to the weights and vertical lines so as to forming lower L/2 number of subfields for M number of vertical lines, wherein N is the number of horizontal pixels, M is the number of vertical lines, L is the number of subfields, and K is the number of bits of the weight data.

To achieve the above object according to a second embodiment of the present invention, there is provided a method of writing N/K groups of non-interlaced video data in an SDRAM used as a frame memory in a PDP type TV receiver, where one frame comprises N × M pixels, each of pixels being sampled with L bits, and then K samples are reordered by L number of weight data, comprising the steps of: a) writing upper L/2 number of weight data with regard to the N/K groups of non-interlaced video data corresponding to M vertical line into respective columns in M row of the first bank according to an incoming order and weights; and b) writing lower L/2 number of weight data with regard to the N/K groups of non-interlaced video data corresponding to M vertical line into respective columns in M row of the second bank according to an incoming order and weights, wherein N is the number of horizontal pixels, M is the number of vertical lines, L is the number of subfields, and K is the number of bits of the weight data.

To achieve the above object according to a second embodiment of the present invention, there is provided a method of reading N/K groups of non-interlaced video data in an SDRAM having a first bank including LM/2K number of columns for storing upper L/2 number of weight data according to weights and a second bank including LM/2K number of columns for storing lower L/2 number of weight data according to weights, used as a frame memory in a PDP type TV receiver, where one frame comprises N × M pixels, each of pixels being sampled with L bits, and then K samples are reordered by L number of weight data, comprising the steps of: a) reading respective weight data from the LM/2K number of columns of the first bank according to the weights and vertical lines so as to forming upper L/2 number of subfields for M number of vertical lines; and b) reading respective weight data from the LM/2K number of columns of the second bank according to the weights and vertical lines so as to forming lower L/2 number of subfields for M number of vertical lines, wherein N is the number of horizontal pixels, M is the number of vertical lines, L is the number of subfields, and K is the number of bits of the weight data.

To achieve the above object according to a third embodiment of the present invention, there is a method of writing N/K groups of non-interlaced video data in an SDRAM used as a frame memory in a PDP type TV receiver, where one frame comprises N × M pixels, each of pixels being sampled with L bits, and then K samples are reordered by L number of weight data, comprising the steps of: a) writing L number of weight data with regard to the N/2K groups of non-interlaced video data corresponding to M vertical line into respective columns in M row of the first bank according to an incoming order and weights; and b) writing L number of weight data with regard to the N/2K groups of non-interlaced video data corresponding to M vertical line into respective columns in M row of the second bank according to an incoming order and weights, wherein N is the number of horizontal pixels, M is the number of vertical lines, L is the number of subfields, and K is the number of bits of the weight data.

To achieve the above object according to a third embodiment of the present invention, there is provided a method of reading N/K groups of non-interlaced video

data in an SDRAM having a first and a second banks, each of banks including LM/2K number of columns for storing L number of weight data according to weights, respectively, used as a frame memory in a PDP type TV receiver, where one frame comprises N × M pixels, each of pixels being sampled with L bits, and then K samples are reordered by L number of weight data, comprising the steps of: a) reading respective weight data from the first bank according to the weights and vertical lines so as to forming L number of subfields for M number of vertical lines; and b) reading respective weight data from the second bank according to the weights and vertical lines so as to forming L number of subfields of M number for vertical lines, wherein N is the number of horizontal pixels, M is the number of vertical lines, L is the number of subfields, and K is the number of bits of the weight data.

BRIEF DESCRIPTION OF THE DRAWINGS

The above object and advantages of the present invention will become more apparent by describing in detail a preferred embodiment thereof with reference to the attached drawings in which:

FIG. 1 is a block diagram of a general AC type color PDP-TV receiver;

FIG. 2 is a block diagram of a memory unit shown in FIG. 1;

FIG. 3 is a diagram showing a data format in a state in which sampled video data are sorted by a 8-bit shift register;

FIG. 4 shows a memory map of a frame memory using an SDRAM in which video data are stored in units of 16 bits according to a first embodiment of the present invention;

FIG. 5 shows a memory map of a frame memory using an SDRAM in which video data are stored in units of 16 bits according to a second embodiment of the present invention; and

FIG. 6 shows a memory map of a frame memory using an SDRAM in which video data are stored in units of 16 bits according to a third embodiment of the present invention.

MODES OF CARRYING OUT THE INVENTION

Hereinbelow, according to a preferred embodiment of the present invention will be described with reference to the accompanying drawings.

FIG. 3 is a diagram showing a data format in a state in which sampled video data are sorted by a 8-bit shift register. D0 to D7 represent MSB to LSB weights of the first to 16th sampled video data, respectively, and D8 to D11 represent MSB to M-3 weights of the 17th to 32th sampled video data, respectively. A video signal corresponding to one frame is sorted, as shown in FIG. 3, and is stored in the first or second frame memory (**230** or **240** of FIG. 2). The number of addressing operations depending on a video mode will now be described. In other words, in the case of a 640 × 480 mode, a memory capacity of 640 × 480 × 8 (= 2,457,600) bits, is required for a channel, e.g., an R channel, and 40 (= 640/16) addressing operations are necessary for 16-bit processing for each line. In the case of a wide mode, that is, a 853 × 480 mode, a memory capacity of 853 × 480 × 8 (= 3,275,520) bits, is required for a channel, and 54 (≅ 853/16) addressing operations are necessary for 16-bit processing.

Next, FIGs. 4 to 6 illustrate first through third embodiments of the present invention of a memory map of a frame memory using an SDRAM for storing video data sorted according to their weights from the data rearrangement portion **210**. First, the SDRAM will be briefly described.

An SDRAM is a dynamic RAM in which all operations are performed in synchronism with basic clocks and has two banks **A** and **B** within one chip and whose internal operation can be controlled by setting a mode register.

The SDRAM is equipped with a burst read mode and a burst write mode. The burst read mode is a mode in which the data of an activated row of an activated bank during consecutive clock cycles are consecutively read. In other words, in a state in which a burst length, a burst sequence and latency are set by the mode register, if an arbitrary read column address of the activated row is input, the video data corresponding to the burst length from the latency can be read without a separate address being input. Using this function, the configuration of the read address generator can be implemented more simply. Also, the burst write mode is a mode

in which consecutive data are written in the activated row of the activated bank of the SDRAM during consecutive clock cycles. In a state in which a burst length, a burst sequence and latency are set by the mode register, if an arbitrary write column address of the activated row is input, the video data are sequentially written in the adjacent column addresses depending on the burst length and the latency. Using this function, the configuration of the write address generator can be implemented more simply.

Referring to FIG. 4, each of the banks **A** and **B** of the SDRAM is divided into four column regions. The bank **A** is divided into MSB to (M-3) storing column regions for storing the MSB to (M-3) weight data corresponding to one frame. The bank **B** is divided into (M-4) to LSB storing column regions for storing the (M-4) to LSB weight data corresponding to one frame. Also, each of the banks **A** and **B** is divided into 480 rows and the video data of one vertical line are stored in the respective lines according to their weights.

According to the first embodiment of a memory map using the SDRAM shown in FIG. 4, since 16-bit video data is written in one matrix address and 40 (= 640/16) addressing operations are necessary for each vertical line in the case of a 640 × 480 mode, at least 40 rows are necessary for each column region, e.g., each of the MSB to LSB column regions. In the case of a 853 × 480 mode, 54 (≅ 853/16) addressing operations are necessary for each vertical line and at least 54 rows are necessary for each column region. In the present invention, it is assumed that 54 columns are provided for implementing the 853 × 480 mode.

If the video data based on the non-interlaced scanning method are classified according to their weights and input, the first to 16th sampled video data of the first vertical line are written in the first MSB, first (M-1), first (M-2) and first (M-3) of the first rows in the bank **A** and in the first (M-4), first (M-5), first (M-6) and first LSB of the first rows in the bank **B** according to their weights. Next, the 17th to 32th sampled video data of the first vertical line are written in the second MSB, second (M-1), second (M-2) and second (M-3) of the first rows in the bank **A** and in the second (M-4), second (M-5), second (M-6) and second LSB of the first rows in the bank **B** according to their weights, respectively. The above-described procedure is

repeated 40 or 54 times in the case of the 640 × 480 mode or the 853 × 480 mode. By the repeated procedures, the video data of the first vertical line can be written in the MSB, (M-1), (M-2) and (M-3) of the first row regions in the bank **A** and in the (M-4), (M-5), (M-6) and LSB of the first row regions in the bank **B** according to their weights, respectively. After the video data of the first vertical line are written according to their weights in the above-described manner, the video data of the second to 480th vertical lines are written by using the above-described method. In detail, the video data of the second to 480th vertical lines are stored in the MSB, (M-1), (M-2) and (M-3) of the first row regions in the bank **A** and in the (M-4), (M-5), (M-6) and LSB of the first row regions in the bank **B** according to their weights, respectively.

If the video data corresponding to one frame are stored on the SDRAM in such a manner as described above, the video data corresponding to one frame are classified according to their vertical lines or weights and stored.

A method of reading the video data written on the SDRAM in the above-described method will now be described with reference to FIG. 4.

Since the video data corresponding to one frame are classified according to their vertical lines or weights and stored, the read operation of the video data is easily performed. First, if a data read signal is input, the data stored in the MSB column region of the first row in the bank **A** are sequentially read and thus the MSB weight data of the first vertical line are all read. Next, the data stored in the MSB row regions of the second to 480th column regions in the bank **A** are sequentially read and thus the MSB weight data of the second to 480th vertical line are all read. In such a reading method, the MSB subframes of one frame can be read.

Here, in a state in which the first row of the bank **A** is activated, if a read row address is input, the burst read operation is allowed. Since various kinds of video data can be read by generating a single read address, the configuration of the read address generator is simplified.

Next, using the same method as that of reading the MSB subframes, the data stored in the (M-1) to (M-3) column regions of the bank **A** are sequentially read, thereby reading the (M-1) to (M-3) subframes, respectively.

Next, the read operation is jumped to the bank **B**, the data stored in the (M-4) column region of the first row in the bank **B** are sequentially read and thus the (M-4) weight data of the first vertical line are all read. In the same manner, the data stored in the (M-4) column region of the second to 480th rows in the bank **B** are sequentially read and thus the MSB weight data of the second to 480th vertical line are all read, thereby reading the (M-4) subframes of one frame.

Next, using the same method as that of reading the (M-4) subframes, the data stored in the (M-5) to LSB column regions in the bank **B** are all read, thereby reading the (M-5) to LSB subframes.

According to the first embodiment of the present invention, in writing the video data based on the non-interlaced scanning method on a frame memory using the SDRAM which is relatively cheap and reading the video data from the frame memory, since a burst read operation is allowed, the configuration of the read address generator can be simplified. Also, the circuit reliability can be improved and the cost can be reduced.

According to the second embodiment of a memory map using an SDRAM shown in FIG. 5, the first to 16th sampled video data of the first vertical line are rearranged according their weights and input as 8 data of a first group, that is, MSB to LSB weights. Among the first group data of the first vertical line, the four upper weight data, that is, MSB to (M-3) weight data, are burst-written in the first to fourth columns of the first row in the bank **A**, and the four lower weight data, that is, (M-4) to LSB weight data, are burst-written in the first to fourth columns of the first row in the bank **B** according to the sequence of their weights. In other words, for the first group data of the first vertical line, if the column addresses of the first rows in the banks **A** and **B** in which the MSB and (M-4) weight data are to be written are given, other weight data are written in the next column addresses of the row addresses for the MSB and (M-4) weight data without separately given addresses. Next, the 17th to 32th sampled video data of the first vertical line are rearranged according to their weights and input as second group data. Among the second group data, the four upper weight data, are burst-written in the fifth to eighth columns of the first row in the bank **A**, and the four lower weight data are burst-written in the fifth to eighth columns of the first row in the bank **B** according to the sequence of their weights.

The above-described operation is repeated up to the 40th group data in the case of 640 × 480 mode and up to the 54th group data in the case of the 853 × 480 mode. Accordingly, among the sampled video data of the first vertical line, the four upper weight data are written in the first row of the bank **A**, and the four lower weight data are written in the first row of the bank **B** according to the sequence of their weights.

Also, the video data of the second to 480th vertical lines are written in the same manner as that of writing the video data of the first vertical line. In the case of the 853 × 480 mode, among the first to 54th group data of the respective vertical lines, the four upper weight data are burst-written in the first to 216th columns of the respective rows in the bank **A**, and the four lower weight data are burst-written in the first to 216th columns of the respective rows in the bank **B**.

If the video data are written on the SDRAM in the above-described manner, since various kinds of data can be written on a single write column address at once, the configuration of the write address generator can be simplified.

A method of reading video data written on the SDRAM in the above-described method for each subframe will now be described with reference to FIG. 5.

If a data read signal is input, the first group MSB weight data of the first row in the bank **A** are read, four columns are jumped, and the procedure of reading the second group MSB weight data is repeated 54 times. In such a manner, the MSB weight data of the first vertical line are all read throughout the first row of the bank **A**. Next, the first to 54th group MSB weight data of the second row in the bank **A** are read. In such a manner, the MSB weight data of the second vertical line are all read from the second row of the bank **A**. By applying the reading method to the respective rows of the bank **A**, the MSB subframes of one frame are all read from the bank **A**. As described above, using the same method as that of reading the MSB subframes of one frame, the (M-1), (M-2) and (M-3) subframes of one frame can be read from the respective rows of the bank **A**.

Next, in the first row of the bank **B**, the first group (M-4) weight data are read, four columns are jumped and the second group (M-4) weight data are read. This procedure is repeated 54 times, thereby reading all the (M-4) weight data of the first vertical line. In the same manner, the (M-4) weight data of the respective

vertical lines are all read from the second to 480th rows of the bank **B**, thereby reading all the (M-4) subframes of one frame. Also, using the method of reading the (M-4) subframes, the (M-5), (M-6) and LSB subframes of one frame can be read from the respective rows of the bank **B**.

According to the second embodiment of the present invention, in writing the video data based on the non-interlaced scanning method on a frame memory using the SDRAM which is relatively cheap and reading the video data from the frame memory, since a burst write operation is allowed, the configuration of the write address generator can be simplified. Also, since a subframe can be read without bank movement, the circuit of the read address generator can be implemented simply. Accordingly, the circuit reliability can be improved and the cost can be reduced.

According to the third embodiment of a memory map using an SDRAM shown in FIG. 6, the first to 16th sampled video data of the first vertical line are rearranged according their weights and input as 8 data of a first group, that is, MSB to LSB weight data. The first group data of the first vertical line are burst-written in the first to 8th columns of the first row in the bank **A** according to the sequence of their weights. In other words, if the column address of the first row in the bank **A** in which the first group MSB weight data are to be written is given, other weight data are written in the next column addresses of the column address for the MSB weight data without separately given addresses. Next, the 17th to 32th sampled video data of the first vertical line are rearranged according to their weights and input as second group data. The second group data are burst-written in the 9th to 16th columns of the first row in the bank **A** according to the sequence of their weights. The above-described operation is repeated up to the 20th group data in the case of 640 × 480 mode and up to the 27th group data in the case of the 853 × 480 mode. Accordingly, half of the sampled video data of the first vertical line are written in the first row of the bank **A** according to the sequence of their sampling operations or weights.

The rest half of the sampled video data of the first vertical lines are burst-written in the first row of the bank **B** in the same manner as described above. In the case of the 853 × 480 mode, each 8 data in the 28th to 54th groups of the first vertical line are burst-written in the first row of the bank **B** in the sequence of their sampling

operations or weights.

The video data of the second to 480th vertical lines are burst-written in the same method as that of writing the video data of the first vertical line. In the case of the 853 × 480 mode, the first to 27th data corresponding to a half of the video data of the respective vertical lines are burst-written in the respective rows of the bank **A**, and the 28th to 54th group data corresponding to the rest half of the video data of the respective vertical lines are burst-written in the respective rows of the bank **B**.

If the video data are written on the SDRAM in the above-described manner, since various kinds of data can be written on a single write column address at once, the configuration of the write address generator can be simplified.

A method of reading video data written on the SDRAM in the above-described method for each subframe will now be described with reference to FIG. 6.

If a data read signal is input, the first group MSB weight data of the first row in the bank **A** are read, eight columns are jumped, and the procedure of reading the second group MSB weight data is repeated 27 times. In such a manner, the 27th group MSB weight data of the first row in the bank **A** are all read. Next, in the bank **B**, the 28th group MSB weight data of the first row in the bank **B** are read, eight columns are jumped, and the procedure of reading the 29th group MSB weight data is repeated 27 times like in the bank **A**. In such a manner, the 54th group MSB weight data of the first row in the bank **B** are all read. The MSB weight data corresponding to the first vertical line are sequentially read by the above-described method.

By applying the same method as that of reading the MSB weight data of the first vertical line, the MSB weight data of the second to 480th vertical line are sequentially read from the second to 480th rows of the banks **A** and **B**, respectively, thereby reading all the MSB subframes of one frame.

Also, using the same method as that of reading the MSB subframe of one frame, the (M-1) subframes of one frame are read in the sequence of the first rows of the banks **A** and **B**, the second rows of the banks **A** and **B**,...and 480th rows of the banks **A** and **B**. In the same manner, the (M-2), (M-3), (M-4), (M-5), (M-6) and LSB subframes are respectively read.

According to the third embodiment of the present invention, in writing the video data based on the non-interlaced scanning method on a frame memory using the SDRAM which is relatively cheap and reading the video data from the frame memory, since a burst write operation is allowed, the configuration of the write address generator can be simplified. Also, since a subframe can be read without bank movement, the circuit reliability can be improved and the cost can be reduced.

While this invention has been described in connection with what is presently considered to be the most practical and preferred embodiments, it is to be understood that the invention is not limited to the disclosed embodiment, but, on the contrary, it is intended to cover various modifications and equivalent arrangements included within the spirit and scope of the appended claims.

WHAT IS CLAIMED IS:

1. A method of writing N/K groups of non-interlaced video data in an SDRAM used as a frame memory in a PDP type TV receiver, where one frame comprises N × M pixels, each of pixels being sampled with L bits, and then K samples are reordered by L number of weight data, comprising the steps of:

a) dividing a first bank of the SDRAM into L/2 number of column regions for storing upper L/2 number of weight data according to weights, respectively;

b) dividing a second bank of the SDRAM into L/2 number of column regions for storing lower L/2 number of weight data according to the weight, respectively; and

c) writing the N/K groups of non-interlaced video data corresponding to M vertical line into respective column regions in M row of the first and second banks according to the weights, wherein N is the number of horizontal pixels, M is the number of vertical lines, L is the number of subfields, and K is the number of bits of the weight data.

2. The method of claim 1, wherein the N/K groups of non-interlaced video data corresponding to respective vertical lines are burst-writtern into respective column regions in respective rows of the first and second banks.

3. A method of reading N/K groups of non-interlaced video data in an SDRAM having a first bank including L/2 number of column regions for storing upper L/2 number of weight data according to weights and a second bank including L/2 number of column regions for storing lower L/2 number of weight data according to weights, used as a frame memory in a PDP type TV receiver, where one frame comprises N × M pixels, each of pixels being sampled with L bits, and then K samples are reordered by L number of weight data, comprising the steps of:

a) reading respective weight data from the L/2 number of column regions of the first bank according to the weights and vertical lines so as to forming upper L/2 number of subfields for M number of vertical lines; and

b) reading respective weight data from the L/2 number of column regions of the second bank according to the weights and vertical lines so as to forming lower L/2 number of subfields for M number of vertical lines, wherein N is the number of

horizontal pixels, M is the number of vertical lines, L is the number of subfields, and K is the number of bits of the weight data.

4. The method of claim 3, wherein respective weight data corresponding to respective subfields are burst-read from the L number of column regions.

5. A method of writing N/K groups of non-interlaced video data in an SDRAM used as a frame memory in a PDP type TV receiver, where one frame comprises N × M pixels, each of pixels being sampled with L bits, and then K samples are reordered by L number of weight data, comprising the steps of:

a) writing upper L/2 number of weight data with regard to the N/K groups of non-interlaced video data corresponding to M vertical line into respective columns in M row of the first bank according to an incoming order and weights; and

b) writing lower L/2 number of weight data with regard to the N/K groups of non-interlaced video data corresponding to M vertical line into respective columns in M row of the second bank according to an incoming order and weights, wherein N is the number of horizontal pixels, M is the number of vertical lines, L is the number of subfields, and K is the number of bits of the weight data.

6. The method of claim 5, wherein the N/K groups of non-interlaced video data corresponding to respective vertical lines are burst-writtern into respective columns in respective rows of the first and second banks.

7. A method of reading N/K groups of non-interlaced video data in an SDRAM having a first bank including LM/2K number of columns for storing upper L/2 number of weight data according to weights and a second bank including LM/2K number of columns for storing lower L/2 number of weight data according to weights, used as a frame memory in a PDP type TV receiver, where one frame comprises N × M pixels, each of pixels being sampled with L bits, and then K samples are reordered by L number of weight data, comprising the steps of:

a) reading respective weight data from the LM/2K number of columns of the first bank according to the weights and vertical lines so as to forming upper L/2 number of subfields for M number of vertical lines; and

b) reading respective weight data from the LM/2K number of columns of the second bank according to the weights and vertical lines so as to forming lower

L/2 number of subfields for M number of vertical lines, wherein N is the number of horizontal pixels, M is the number of vertical lines, L is the number of subfields, and K is the number of bits of the weight data.

8. The method of claim 7, wherein respective weight data corresponding to respective subfields are burst-read from the LM/2K number of columns.

9. A method of writing N/K groups of non-interlaced video data in an SDRAM used as a frame memory in a PDP type TV receiver, where one frame comprises N × M pixels, each of pixels being sampled with L bits, and then K samples are reordered by L number of weight data, comprising the steps of:

a) writing L number of weight data with regard to the N/2K groups of non-interlaced video data corresponding to M vertical line into respective columns in M row of the first bank according to an incoming order and weights; and

b) writing L number of weight data with regard to the N/2K groups of non-interlaced video data corresponding to M vertical line into respective columns in M row of the second bank according to an incoming order and weights, wherein N is the number of horizontal pixels, M is the number of vertical lines, L is the number of subfields, and K is the number of bits of the weight data.

10. The method of claim 9, wherein the N/K groups of non-interlaced video data corresponding to respective vertical lines are burst-writtern into respective columns in respective rows of the first and second banks.

11. A method of reading N/K groups of non-interlaced video data in an SDRAM having a first and a second banks, each of banks including LM/2K number of columns for storing L number of weight data according to weights, respectively, used as a frame memory in a PDP type TV receiver, where one frame comprises N × M pixels, each of pixels being sampled with L bits, and then K samples are reordered by L number of weight data, comprising the steps of:

a) reading respective weight data from the first bank according to the weights and vertical lines so as to forming L number of subfields for M number of vertical lines; and

b) reading respective weight data from the second bank according to the weights and vertical lines so as to forming L number of subfields of M number for

vertical lines, wherein N is the number of horizontal pixels, M is the number of vertical lines, L is the number of subfields, and K is the number of bits of the weight data.

12. The method of claim 11, wherein respective weight data corresponding to respective subfields are burst-read from the LM/2K number of columns.

FIG. 1

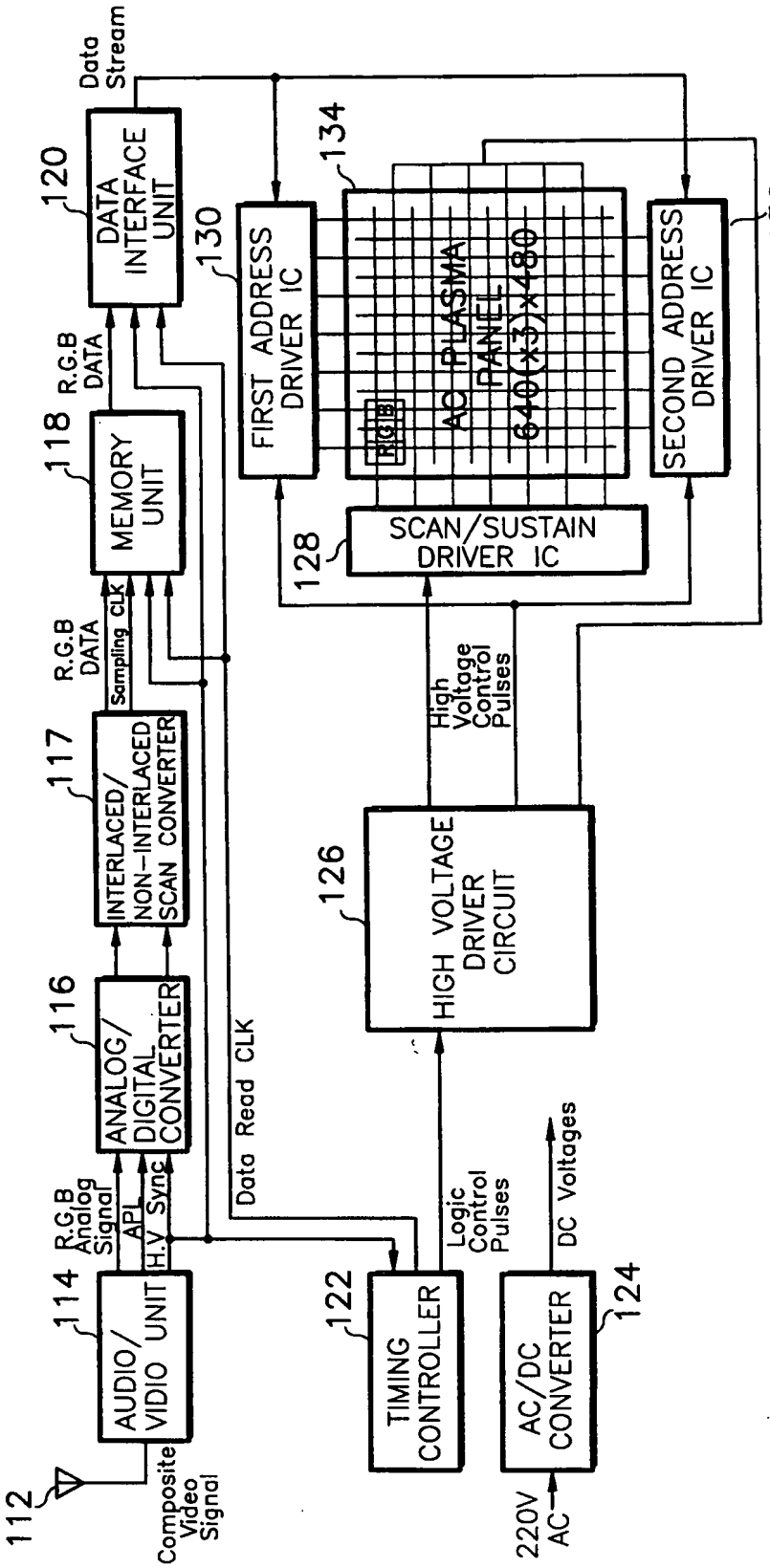

112
Composite Video Signal
AUDIO/ VIDIO UNIT
114
R.G.B Analog Signal
APL
H.V Sync
ANALOG/ DIGITAL CONVERTER
116
INTERLACED/ NON-INTERLACED SCAN CONVERTER
117
R.G.B DATA
Sampling CLK
MEMORY UNIT
118
R.G.B DATA
DATA INTERFACE UNIT
120
Data Stream
TIMING CONTROLLER
122
Logic Control Pulses
Data Read CLK
AC/DC CONVERTER
124
DC Voltages
220V AC
HIGH VOLTAGE DRIVER CIRCUIT
126
High Voltage Control Pulses
SCAN/SUSTAIN DRIVER IC
128
FIRST ADDRESS DRIVER IC
130
AC PLASMA PANEL 640(x3)x480
134
R.G.B
SECOND ADDRESS DRIVER IC
132

FIG. 2

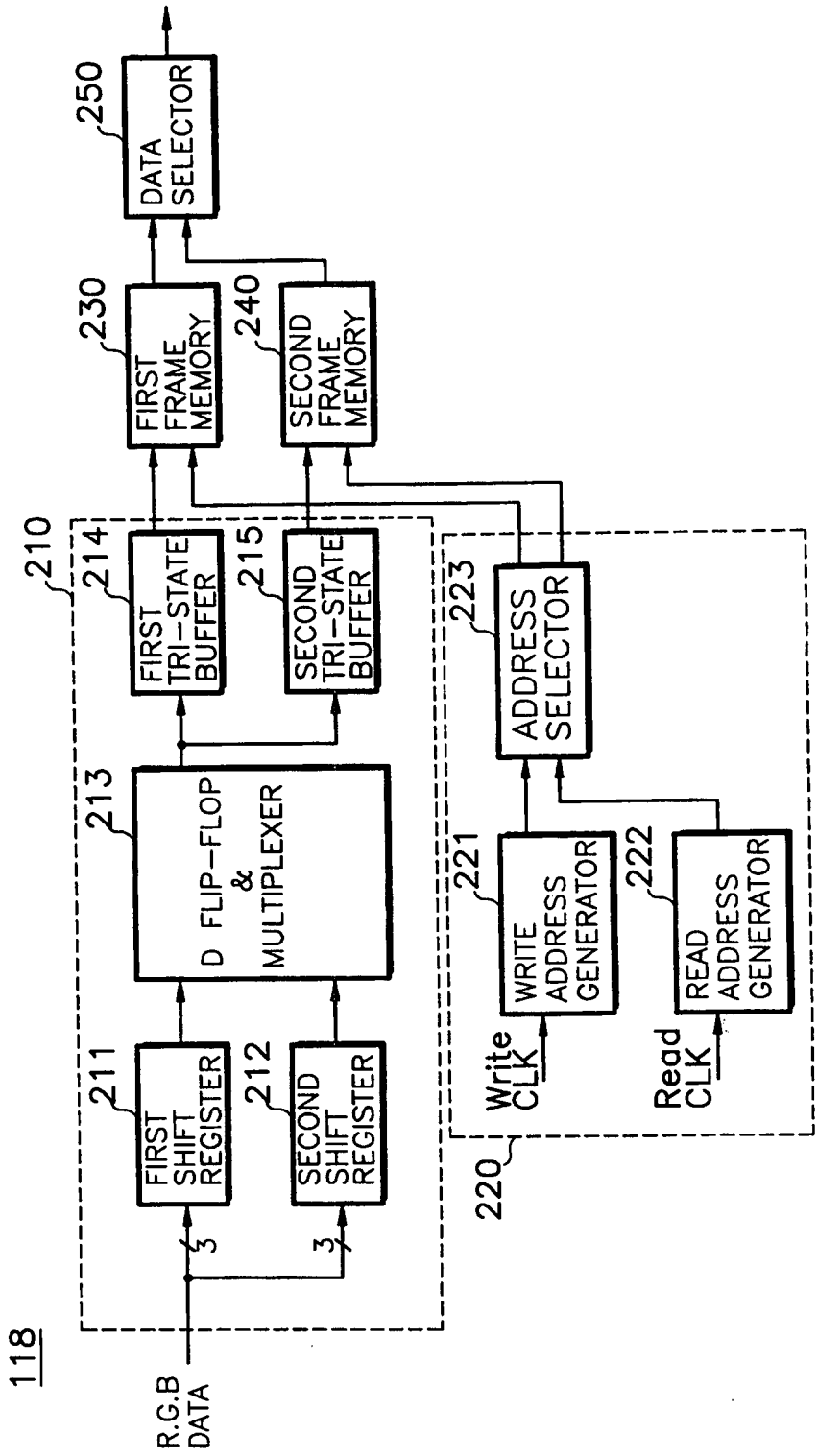

118
R.G.B DATA
3
3
210
211
FIRST SHIFT REGISTER
212
SECOND SHIFT REGISTER
213
D FLIP-FLOP & MULTIPLEXER
214
FIRST TRI-STATE BUFFER
215
SECOND TRI-STATE BUFFER
220
221
WRITE ADDRESS GENERATOR
222
READ ADDRESS GENERATOR
223
ADDRESS SELECTOR
Write CLK
Read CLK
230
FIRST FRAME MEMORY
240
SECOND FRAME MEMORY
250
DATA SELECTOR

FIG. 3

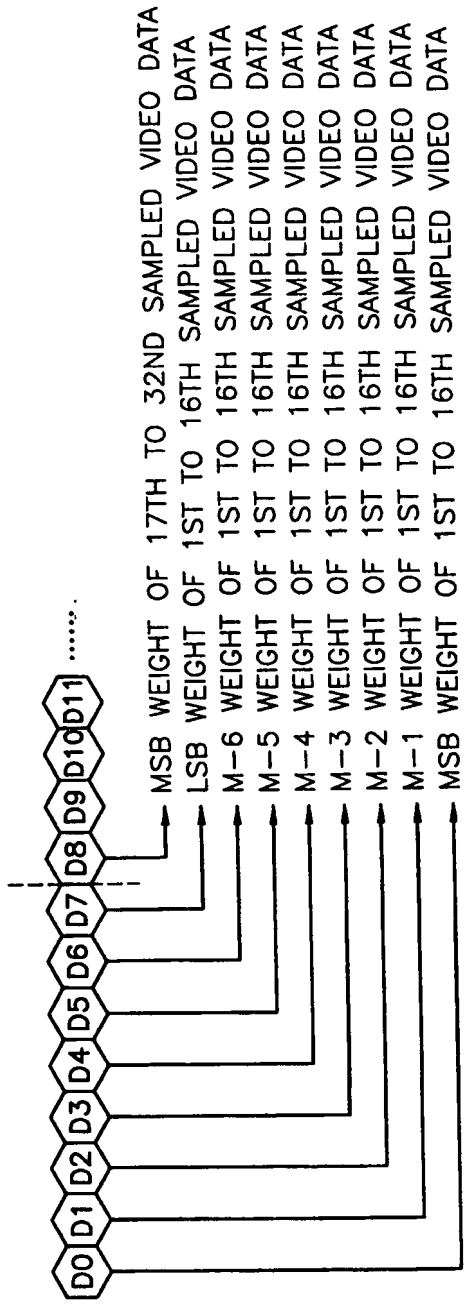

D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
.....
MSB WEIGHT OF 17TH TO 32ND SAMPLED VIDEO DATA
LSB WEIGHT OF 1ST TO 16TH SAMPLED VIDEO DATA
M-6 WEIGHT OF 1ST TO 16TH SAMPLED VIDEO DATA
M-5 WEIGHT OF 1ST TO 16TH SAMPLED VIDEO DATA
M-4 WEIGHT OF 1ST TO 16TH SAMPLED VIDEO DATA
M-3 WEIGHT OF 1ST TO 16TH SAMPLED VIDEO DATA
M-2 WEIGHT OF 1ST TO 16TH SAMPLED VIDEO DATA
M-1 WEIGHT OF 1ST TO 16TH SAMPLED VIDEO DATA
MSB WEIGHT OF 1ST TO 16TH SAMPLED VIDEO DATA

FIG. 4

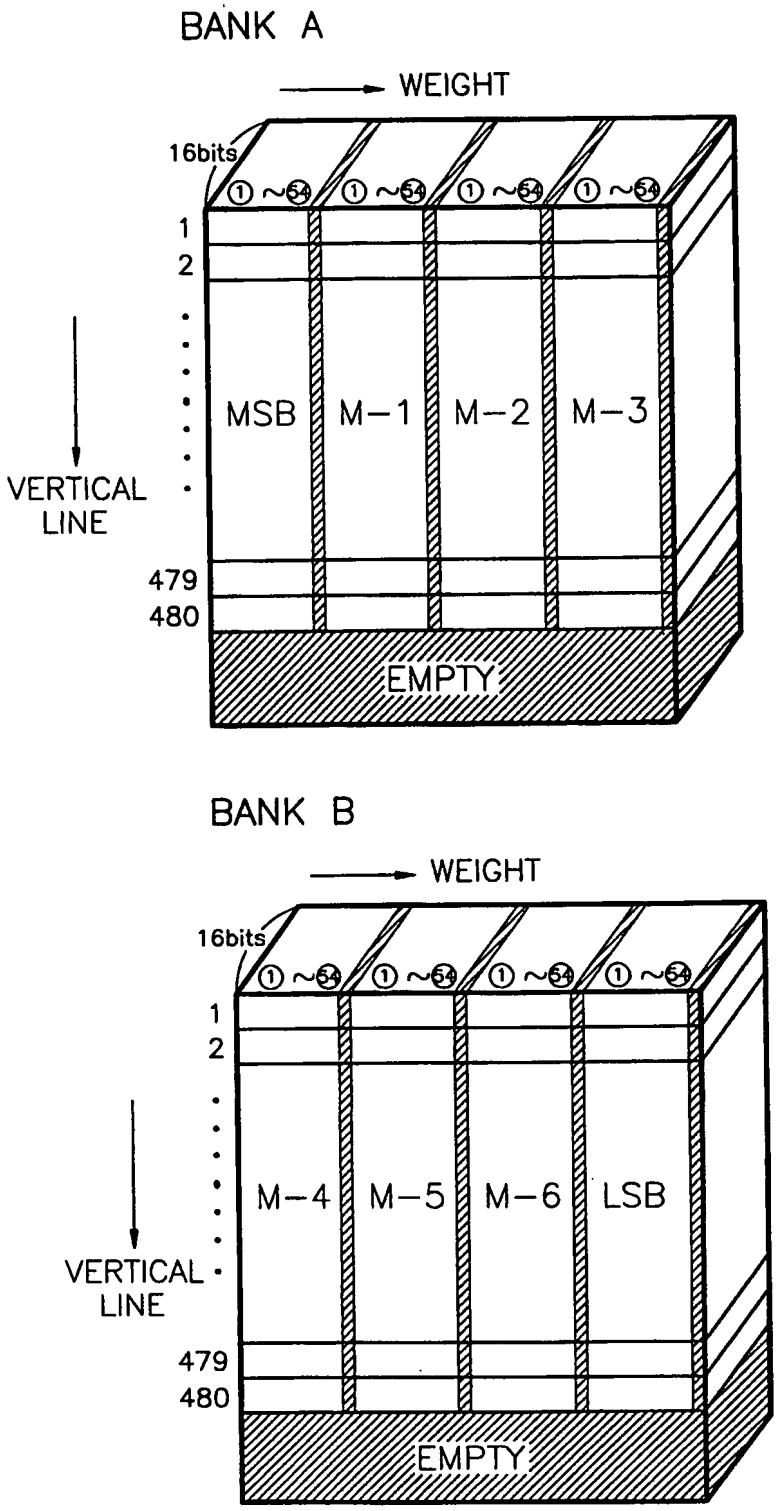

BANK A
WEIGHT
16bits
① ~54
1
2
MSB
M-1
M-2
M-3
VERTICAL LINE
479
480
EMPTY
BANK B
WEIGHT
16bits
① ~54
1
2
M-4
M-5
M-6
LSB
VERTICAL LINE
479
480
EMPTY

FIG. 5

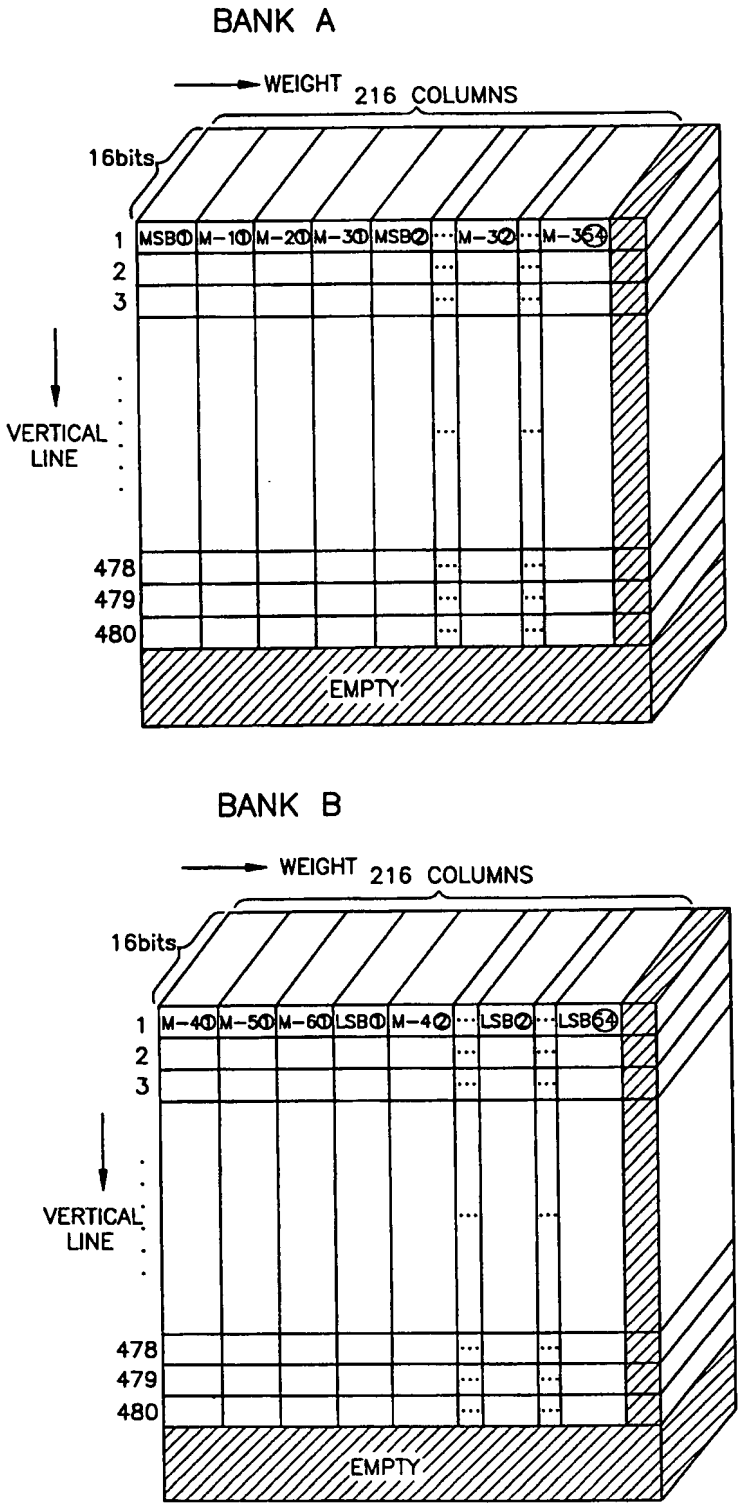
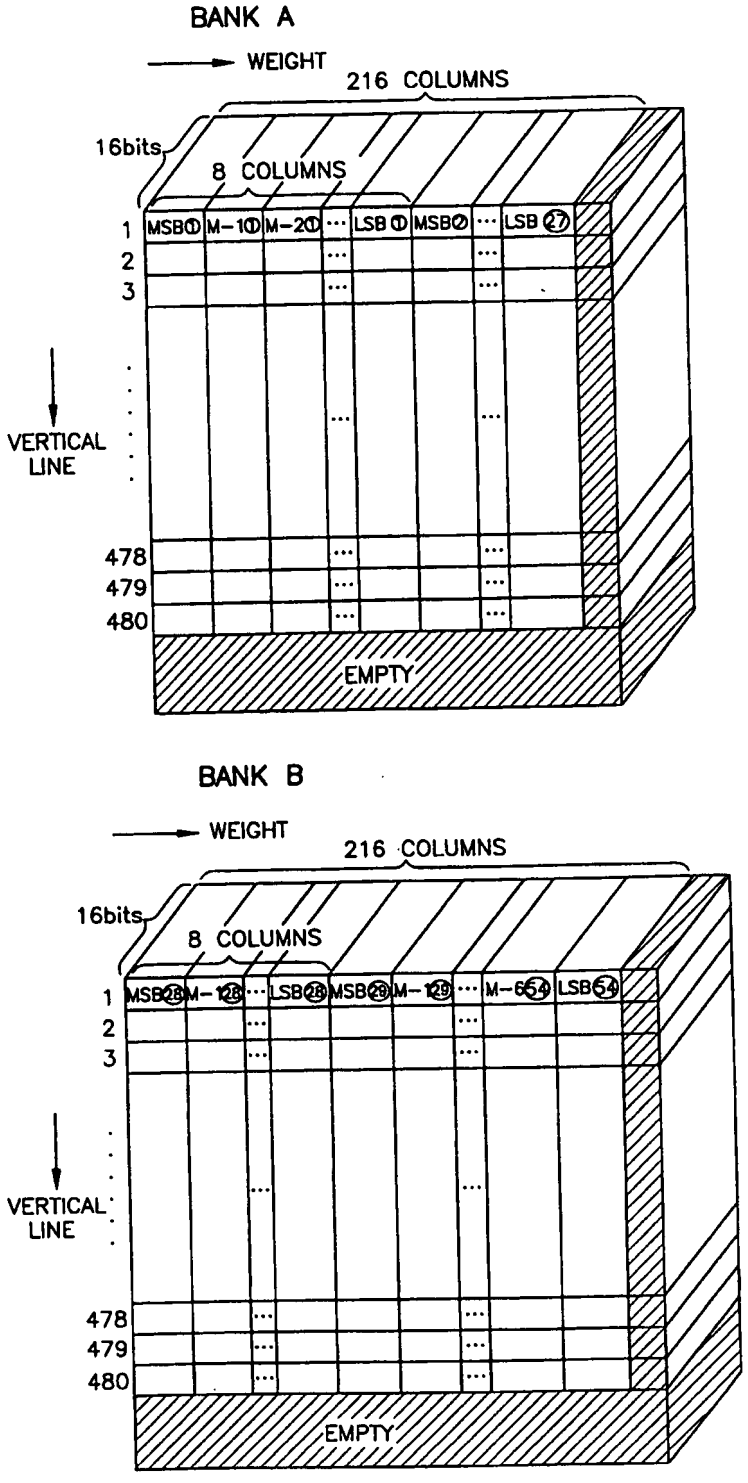

BANK A
WEIGHT
216 COLUMNS
16bits
1
2
3
478
479
480
MSB①
M-1①
M-2①
M-3①
MSB②
M-3②
M-36④
VERTICAL LINE
EMPTY
BANK B
WEIGHT
216 COLUMNS
16bits
1
2
3
478
479
480
M-4①
M-5①
M-6①
LSB①
M-4②
LSB②
LSB64④
VERTICAL LINE
EMPTY

FIG. 6


BANK A
WEIGHT
216 COLUMNS
16bits
8 COLUMNS
1
2
3
MSB①
M-10①
M-20①
LSB①
MSB②
LSB㉗
VERTICAL LINE
478
479
480
EMPTY
BANK B
WEIGHT
216 COLUMNS
16bits
8 COLUMNS
1
2
3
MSB㉘
M-128
LSB㉘
MSB㉘
M-129
M-654
LSB54
VERTICAL LINE
478
479
480
EMPTY

INTERNATIONAL SEARCH REPORT

International application No.
PCT/KR 99/00008

A. CLASSIFICATION OF SUBJECT MATTER

IPC[6]: G 09 G 3/28, H 04 N 5/66

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

IPC[6]: G 09 G 3/28; H 04 N 5/66, 7/24, 7/30, 7/32

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

WPI

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	Database PAJ in EPOQUE: Patent Abstracts of Japan, Vol. 96, No. 11, 1996, JP 8-186 826A (GRAPHICS COMMUN.LAB.) 29 November 1996.	1,3,5,7,9,11
A	GB 2 303 989 A (SAMSUNG ELECTRONICS) 05 March 1997 (05.03.97), fig. 4; claims 1-6.	1,3,5,7,9,11
A	US 5 684 753 A (DOLAIT et al.) 04 November 1997 (04.11.97), claims 1-10.	1,3,5,7,9,11

☐ Further documents are listed in the continuation of Box C.

☒ See patent family annex.

* Special categories of cited documents:
„A" document defining the general state of the art which is not considered to be of particular relevance
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„O" document referring to an oral disclosure, use, exhibition or other means
„P" document published prior to the international filing date but later than the priority date claimed
„T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
„X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone
„Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art
„&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
30 April 1999	14 May 1999 (14.05.99)
Name and mailing adress of the ISA/AT Austrian Patent Office Kohlmarkt 8-10; A-1014 Vienna Facsimile No. 1/53424/535	Authorized officer Fussy Telephone No. 1/53424/328

Form PCT/ISA/210 (second sheet) (July 1998)

INTERNATIONAL SEARCH REPORT

Information on patent family members

International application No.
PCT/KR 99/00008

Im Recherchenbericht angeführtes Patentdokument Patent document cited in search report Document de brevet cité dans le rapport de recherche	Datum der Veröffentlichung Publication date Date de publication	Mitglied(er) der Patentfamilie Patent family member(s) Membre(s) de la famille de brevets	Datum der Veröffentlichung Publication date Date de publication
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		GB A0 9615911	11-09-1996
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		US A 5680368	21-10-1997
		US A 5680369	21-10-1997
		US A 5680370	21-10-1997
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		US A 5805518	08-09-1998